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EXAMINER	
WONG, LINDA	

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2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/092,758	NGUYEN ET AL.
	Examiner	Art Unit
	Linda Wong	2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 7/3/2007 have been fully considered but they are not persuasive.

   a. The applicant contends

   "Claims 1-3, 5-7, and 9 were rejected for anticipation in view of Marko. Claims 4 and 8 were rejected as unpatentable over Marko in view of Carlson. Applicant requests reconsideration. Applicant extends appreciation to the examiner for the thorough examination, and particularly the detailed claim analysis, as that will focus this case. However, it should be noted that that analysis repetitively used the term "pulses" in connection with the teachings of Marko, yet, Marko does not teach "pulses" in any regard with respect to lead and lag incrementation, but rather teaches the use of "transitions". Marko never discusses in any regard the use of pulses for lead and lag determination, yet the claim analysis is saturated with references to "pulses" taught by Marko, which are clearly not taught. This characterization of Marko's transitions as if the same of the applicant's pulses is an unfair characterization in an anticipation rejection, and suggests a bias towards forbidden hindsight reconstruction. Marko never taught the use of pulses for lead and lag incrementation. New claim i0 was added to recite that the baseband waveform signal as claimed has zero crossings from which pulses are generated. New claim ii was added to recite that the baseband waveform signal that encodes a digital bit stream, is modulated using various modulation methods. Marko's system does not generate pulses, and does not generate pulses from zero crossings, nor generate pulses from zero crossings from baseband signals generated from conventional communication modulation methods. Claims 10 and 11 further distinguish the present invention from Marko, and particularly as now newly claimed."

   The examiner respectfully disagrees. The applicant contends Marko fails to disclose "pulses", instead discloses "transitions". A pulse will transition from one point to another. Fig. 5 shows a diagram of the transitions of the pulses. Thus, since Marko determines the characteristics of the transitions, Marko would also determine the characteristics of the pulses. Furthermore, the limitation recites "data transition pulses". As shown in Fig. 5, Marko determines the characteristics of the "data transition pulses".

   b. The applicant further contends

   "Marko does not anticipate the present invention, at least, because: i) Marko uses a recovered data signal as the input and are not the baseband waveform encoding a data bit stream; 2)

because Marko early and late increments are based upon transitions of the recovered data signal and not based on pulses generated from the baseband waveform; and 3) because the phase error in Marko is determined from transitions and not from pulses. The RX data, that is, the recovered data signal, in Marko, is not a wideband waveform encoding a digital bit stream, as it is the data stream itself. The early and late increments, in Marko, are based on recovered data transitions and recovered clock transitions, and not on wideband waveform transition pulses and adjusted timing pulses. The phase error is determined, in Marko, by differences between the recovered data signal and the recovered clock, and not on differences between wideband zero crossing transition pulses and adjusted timing pulses. Significant teachings, with underline emphasis added, of Marko, are here set forth in full, for convenience."

The examiner respectfully disagrees. Regarding point I), Marko discloses a received baseband signal, wherein the received signal would be a self clocked signal. The rejection below has explained in detail the examiner's interpretation. Regarding point 2), as discussed above, transitions occur in pulses, thus since Marko determines the characteristics of the transitions, Marko would also determine the characteristics of the pulses. Regarding point 3), as discussed above, transitions occur in pulses. Since Marko determines the error in the transitions, the error would also exist in the pulses. The applicant also indicates the recovered data signal as disclosed by Marko "is not a wideband waveform encoding a digital bit stream." Such a limitation is not recited in the claim, thus such limitation has not been considered.

c. The applicant further contends

"Marko's transitions and applicant's pulses solve different problems associated with different designs. Marko's first translates the baseband waveform signal into a recovered data signal having jittering associated with bit boundary quantization detection, into a non-jittering digital recovered signal not having any zero crossings. Marko uses the 1/32 bit period boundary quantization for determining time of transitions. This 1/32 bit period is a discrete sampling, whereas the pulse detection from a baseband signal having zero crossings has a continuum sampling of infinite precision, though subject to false triggering when the baseband signal is noisy about the zero crossings. Hence, the present invention compares baseband waveform signal zero crossing transition pulses with adjusted pulses, and in the event of false triggering, ignores double triggers or no triggers. Marko's 1/32 bit period transition time quantization can not be as precise as an analog continuum sampling through a zero crossing, and does not have the problem of generating and comparing good and false pulses."

The examiner respectfully disagrees. The applicant compares the invention of Marko as differing from the applicant's invention, wherein the difference between the two inventions lies in the applicant's invention "compares baseband waveform signal zero crossing transition pulses with adjusted pulses". Such a limitation is not found within claim 1, but is only found within claim 10. Since claim 10 is a new submitted claim, a prior art rejection has not been completed in the office action mailed 12/29/2006. The examiner has indicated a prior art rejection as indicated below. Please review the rejection below.

d. The applicant further contends

> "Marko's design is fundamentally different from the present invention. Marko first digitizes the incoming baseband waveform signal into an RX data recovered signal square wave extending from only a zero level to only a high level. Then, Marko seeks to determine the phase error based on time differences between transitions of the RX data recovered signals and the recovered clock. The present invention does not convert the incoming baseband waveform signal into a like high and low digital recovered data signal prior to determining the phase errors. In Figure 1, the data detector actually receives the baseband waveform signal. The data detection is had by applying the adjusted pulses directly to the baseband waveform signal for only then generating the digital bit stream, whereas Marko's data detector applies recovered clock transitions to the RX recovered data signal to generate the data bit stream. The high-order architecture of Marko is thereby different in approach, and thereby, not only does not suggest the claimed combination, but also, teaches contrary to the present invention, and thus, Marko is strong evidence of nonobviousness."

The examiner respectfully disagrees. Marko et al discloses "the instantaneous recovered timing of the wide bandwidth recovered clock 106 with respect to receive baseband data timing 102 are compared to a reference 104. The first order wideband DPLL recover timing 106 can track the instantaneous baseband timing closely and thus track the received data transitions well within

predetermined error limits 108 for muting." (Col. 1, lines 30-36) Marko indicates the recovered timing is based on the baseband data timing, wherein the phase detector compares the recovered timing with respect to the receive baseband data timing. Since the recovered timing is based on the baseband data timing, the phase error is based on the baseband data timing signal, thus the error produced by the phase detector would be the difference between the baseband data timing signal and the adjusted timing signal.

e. The applicant further contends

> "Marko does not anticipate the present invention because 1) Marko uses a recovered data signal as the input and not the baseband waveform encoding a data bit stream; 2) because Marko early and late increments are based upon transitions of the recovered data signal and not based on pulses generated from the baseband waveform; and 3) because the phase error in Marko is determined from transitions and not from pulses. Marko does not suggest the present invention, at least, because: 1) Marko teaches away form the present invention by firstly digitizing the baseband waveform into a recovered data signal in advance of data detection, which is completely contrary to applicant's data detection directly upon the baseband waveform signal encoding the digital bit stream using pulses generated from that baseband waveform, 2) because Marko's quantization of the modulated baseband waveform signals into the data recovered signals, which then used for data detection, and which injects jitter errors due to discrete 1/32 bit boundaries quantization, is counter-intuitive to the use of a continuum flowing through zero crossings of modulated baseband waveform signals. The combination of Marko and Carlson thereby becomes largely irrelevant respecting in these aspects. Applicant requests allowance of claims."

The examiner respectfully disagrees. Regarding points 1,2, and 3, the examiner has provided a rebuttal for such remarks. Please see refer to the related rebuttal above. Regarding point 1, where the applicant contends Marko teaches away from the invention, the examiner has provided a rebuttal. Please see refer to the related rebuttal above. Regarding point 2, where the applicant remarks on the motivation for combination of Marko and Carlson, the applicant remarks on zero crossings found within the baseband signal. Such a limitation

is not found within claim 1 and only found in claim 10. Since claim 10 is a new claim, a prior art rejection has not yet been provided. Please see the rejection as stated below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-3,5-7,9** are rejected under 35 U.S.C. 102(b) as being anticipated by Marko et al (US Patent No.: 5463351).

   a. **Claim 1**,

      i. Marko et al discloses:

         - A data transition generator (Fig. 9b, label 948) for generating data transition pulses from a received baseband signal (Col. 7, lines 30-33, Col. 1, lines 55-62), wherein the received signal is inherently a self clocked signal. The received signals are further transmitted/received by a receiver front end coupled to a time division multiplexor for providing time division multiplexed framed digital signals. Framed digital signals would inherently comprise multiple or many bits within a frame or period. (Col. 2, lines 51-67 and Col. 3, lines 1-5) Since the data transition pulses are generated from the received signals, wherein the

received signals contain bits within a frame, the data transition pulses are in synchronous with the received signal.

- A phase detector (Fig. 9b, label 950) for comparing the data transition pulses (Fig. 9b, label 948) with the adjusted timing pulses (Fig. 9b, label wide BW recovered clock) for generating early and late signals (Fig. 9b, labels early/late), wherein the early and late signals are inherently generated when the data transition pulses (Fig. 9b, output from label 948) leads or lags the adjusted timing pulses (Fig. 9b, label wide bw received clock).
- A counter or random walk counter (Fig. 9b, label 956) for counting the early signals and lag signals (Fig. 9b, label 952), wherein multiple frames of data is received (Col. 2, lines 61-67 and Col. 3, lines 1-5), the count would be performed for a plurality of bit periods.
- A threshold comparator (Fig. 9b, label 966) for comparing the count outputted by the counter (Fig. 9b, label 956) with a predetermined threshold (Fig. 9b, label 964) and
- A timing pulse delay adjustor (Fig. 9b, labels 970,974,976 and Fig. 4, label 436) for adjusting the timing pulse delay communicated to the phase detector (Fig. 9b, label 950) for adjusting the phase of the adjusted timing pulses (Col. 4, lines 18-39), which inherently adjusts the time or delays the pulses. The adjustment to the timing pulses occurs when the count exceeds the predetermined threshold. (Col. 9, lines 15-

30) The phase detector synchronizes the delayed or adjusted timing pulses with the data transition pulses (Fig. 9b, label 950), wherein the data transition pulses are generated from the received signals. The received signals contain bits within a frame and multiple frames are received. (Col. 2, lines 51-67 and Col. 3, lines 1-5)

b. **Claim 2**, Marko et al discloses a data detector (Fig. 9b, label 948), wherein the transition detector detects and generates transitions by sampling the received signal. (Col. 8, lines 62-67)

c. **Claim 3**, Marko et al discloses "the predetermined wide loop BW value 964 set by the controller 962 is preferably less than 20...", which indicates the controller sets the value of the predetermined threshold or predetermined wide loop BW value on some value that is preferably less than 20. Such a value can be selected to be any value as long as the above criterion is maintained. (Col. 9, lines 24-29)

d. **Claim 5,**

i. Marko et al teaches

- "a count magnitude generator for generating the magnitude count from the running count," (see the output magnitude from the early/late count Fig. 9, label 960)
- "the magnitude count being fed to the threshold count comparator for determining when the running count exceeds the predetermined first

threshold count value, and" (see input to a comparator, which compares the count with a threshold (Fig. 9, label 966)

- "a count sign clipper for generating a count sign from the running count, the count sign being fed to the timing pulse delay adjustor for generating a timing pulse delay to adjust the adjusted timing pulses," (see sign outputted from label 956 in Fig. 9b)
- "the sign count for increasing the timing pulse delay when the data transition pulses arrive late relative to the adjusted timing pulses and for decreasing the timing pulse delay when the data transition pulses arrive early relative to the adjusted timing pulses" (see Col. 3, lines 55-66 which explains counts up for a lead and down for lag)

e. **Claim 6**,

i. Marko et al discloses

- "a data transition pulse generator for generating the data transition pulses" (see Fig. 9b, label 948)
- " a timing delay for delaying reference timing pulses into the adjusted timing pulse" (see Fig. 9b, labels 970,975,978)
- "a lead and lag generator for generating lead and lag signals for early and late arrivals of the data transition pulses relative to the adjusted timing pulses" (see Fig. 9b, labels 952 and 950).

f. **Claim 7** recites similar limitations regarding the "data transition pulse generator ...", "timing delay ...", "data transition pulse counter ...", and "lead and lag

generator ..." as claim 6. The rejection for claim 7 regarding the limitations stated above is as stated for claim 6.

i. Claim 6 does not recite the limitation "when one and only one data transition pulse occurs within each search window following an adjusted timing pulse".

- Marko et al discloses receiving input bits within a frame, wherein the received signal is used within the transition detector and the phase detector (Fig. 9b, labels 948,950 and Col. 2, lines 51-67 and Col. 3, lines 1-5). Thus, the phase detector would detect a lead or lag between the data transition pulses (Fig. 9b, output from label 948) and the adjusted timing pulses (Fig. 9b, labels 970,974,980 and Fig. 4, label 436) would be detected within the frame of the received signal.

g. **Claim 9**, Regarding the limitation "the random walk counter sums the lead signals and lag signals as the running count", Marko et al discloses an early/late accumulator for summing the number of lead and lags. (Fig. 9b, label 956)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 4,8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Marko et al (US Patent No.: 5463351) in view of Carlson (US Patent No.: 6167526).

a. **Claim 4,**

i. Marko et al teaches "a threshold count value selector for selecting the first threshold count value" by disclosing a controller for selecting a value less than 20 to be used by the comparator (Fig. 9b, label 962,966 and Col. 9, lines 24-29 and please refer to the rejection of claim 3 for further explanation of the threshold selector)

ii. Marko et al fails to discloses "an adaptive means for monitoring the rate at which the timing pulse delay is adjusted, the threshold value count selector adaptively selecting different first threshold count values when the adjustment rate exceeds a predetermined rate being a second threshold count value".

- Carlson discloses a timing system updating or selecting the parameters of a window based on the predetermined value is less than the count of the early/late pulses. (Col. 3, lines 45-52) and an adaptive means, which updates or selects a new threshold when the predetermined rate is less than the adjustment rate or the second threshold count value. (Col. 3, lines 45-52, Fig. 4, Fig. 3, labels 380,390,x0-x3)
- Thus, it would be obvious to one skilled in the art to incorporate Carlson's invention into Marko et al's invention to provide more robust detection circuit, which is "less susceptible and sensitive to noise error."

b. **Claim 8** recites similar limitations regarding the "data transition pulse generator ...", "timing delay ...", "data transition pulse counter ...", and "lead and lag generator ..." as claim 7. The rejection for claim 8 regarding the limitations stated above is as stated for claim 7.

i. **Claim 7** does not recite the limitation "a window delay for delaying the data transition pulses by half of a search window to center the data transition pulses within respective search windows".

- Carlson discloses a window detection unit (Fig. 3, label 308), wherein the windows of the early and late detectors (Fig. 3, labels 320 and 322) is controlled by unit label 308. Thus, when one data transition pulse is detected to be either early or late within the window, the counter is increased or decreased (Fig. 3, label 370) and the adjusted timing pulses are produced. (Fig. 3, labels 308 and Col. 4, lines 26-32)

4. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable by Marko et al (US Patent No.: 5463351) in view of Ishizu (US Patent No.: 5661765).

a. **Claim 10**,

i. Marko et al disclose

- A data transition generator (Fig. 9b, label 948) for generating data transition pulses from a received baseband signal (Col. 7, lines 30-33, Col. 1, lines 55-62), wherein the received signal is inherently a self clocked signal. The received signals are further transmitted/received by

a receiver front end coupled to a time division multiplexor for providing time division multiplexed framed digital signals. Framed digital signals would inherently comprise multiple or many bits within a frame or period. (Col. 2, lines 51-67 and Col. 3, lines 1-5) Since the data transition pulses are generated from the received signals, wherein the received signals contain bits within a frame, the data transition pulses are in synchronous with the received signal.

- A phase detector (Fig. 9b, label 950) for comparing the data transition pulses (Fig. 9b, label 948) with the adjusted timing pulses (Fig. 9b, label wide BW recovered clock) for generating early and late signals (Fig. 9b, labels early/late), wherein the early and late signals are inherently generated when the data transition pulses (Fig. 9b, output from label 948) leads or lags the adjusted timing pulses (Fig. 9b, label wide bw received clock).
- A counter or random walk counter (Fig. 9b, label 956) for counting the early signals and lag signals (Fig. 9b, label 952), wherein multiple frames of data is received (Col. 2, lines 61-67 and Col. 3, lines 1-5), the count would be performed for a plurality of bit periods.
- A threshold comparator (Fig. 9b, label 966) for comparing the count outputted by the counter (Fig. 9b, label 956) with a predetermined threshold (Fig. 9b, label 964) and

- A timing pulse delay adjustor (Fig. 9b, labels 970,974,976 and Fig. 4, label 436) for adjusting the timing pulse delay communicated to the phase detector (Fig. 9b, label 950) for adjusting the phase of the adjusted timing pulses (Col. 4, lines 18-39), which inherently adjusts the time or delays the pulses. The adjustment to the timing pulses occurs when the count exceeds the predetermined threshold. (Col. 9, lines 15-30) The phase detector synchronizes the delayed or adjusted timing pulses with the data transition pulses (Fig. 9b, label 950), wherein the data transition pulses are generated from the received signals. The received signals contain bits within a frame and multiple frames are received. (Col. 2, lines 51-67 and Col. 3, lines 1-5)

ii. Marko et al fails to disclose "a pulse detector for generating data transition pulses from the zero crossings of the baseband signal waveform".

iii. Ishizu discloses such a limitation. (Col. 3, lines 10-16 disclose the zero crossing information found within the signal is determined for significant/insignificant or lead/lag. Col. 2, lines 35-37 discloses "A sign bit (MSB: {1,0}) represented in the form of a baseband waveform, of the output of the demodulator 2 is inputted to the phase comparator 3." Fig. 18(a) shows a diagram of a sample of a baseband signal. Fig. 16, label 3 shows a phase comparator.) It would have been obvious to one skilled in the art to incorporate a pulse detector for generating data transition pulses from the

zero crossings of the baseband signal waveform" as disclosed by Ishizu into Marko et al's invention so to maintain phase synchronization.

5. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable by Marko et al in view of Ishizu as applied to claim 10, further in view of Downey et al (US Patent No.: 5553081).
    a. **Claim 11**, Marko et al in view of Ishizu fails to disclose "the baseband waveform signal having zero crossings encodes the digital bit stream using a modulation method selected from the group consisting of BPSK, QPSK, GMSK, 16-QAM and 64-QAM". Downey et al discloses such a limitation. (Col. 18, lines 43-44, lines 45-46) It would have been obvious to one skilled in the art to modulate or demodulate as disclosed by Downey et al and incorporate such a scheme into Marko et al in view of Ishizu's invention so to provide a demodulated/modulated signal based on such modulation scheme.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
    a. Surie et al (US Patent No.: 4599735)
    b. Fujii (US Patent No.: 5349309)
    c. Kuramatsu (US Patent No.: 5440298).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong

David Payne
DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER